

Attorney
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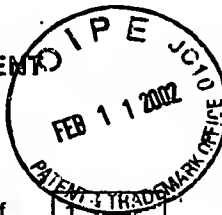
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284032

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**INFORMATION DISCLOSURE STATEMENT
BY APPLICANT**



Applicant: YAMADA et al

Appln. No.: 09/993,967

Filing Date: November 27, 2001

Date: February 11, 2002

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of

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Examiner:

Group Art Unit: 2812

U.S. PATENT DOCUMENTS

Examiner's Initials*	Document Number	Date MM/YYYY	Name (Family Name of First Inventor)	Class	Sub Class	Filing Date (if appropriate)
	AR					
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							Enclosed	No	Enclose	No
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OTHER (Including in this order Author, Title, Periodical Name, Date, Pertinent Pages, etc.)

YR	T. Hamamoto et al., "well concentration: A Novel Scaling Limitation Factor derived from DRAM, Retention Time and Its Modeling" IEDM Tec. Dig., P915-918			
ZR				
AAR				
BBR				

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FORM PTO-1449 (modified)
 To: U.S. Department of Commerce
 (PW FORM PAT-1449)
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10872 U.S. PTO
09/993967



INFORMATION DISCLOSURE STATEMENT BY APPLICANT

Applicant: YAMADA et al.

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Date: November 27, 2001

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FOREIGN PATENT DOCUMENTS

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ML	WR	U. Gruening, et al., IEDM Technical Digest, "A Novel Trench DRAM Cell with a VERTICAL Access Transistor and Buried STrap (VERI BEST) for 4Gb/16Gb", 1999, pp. 25-28			
ML	XR	C. J. Radens, et al., IEDM Technical Digest, "An Orthogonal 6F2 Trench-Sidewall Vertical Device Cell for 4Gb/16Gb DRAM", 2000, pp. 349-352			
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	ZR				
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